a carry circuit coupled to the outputs of the shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuit; and
a second or more shift bar circuits cascaded together to produce a modulo sum and one or more carry bits; an encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

60.(Original) The reconfigurable matrix multiplier circuit of claim 59 wherein the shift bar circuits further comprise full adders coupled to the output the encoder circuits.

REMARKS

In an office action mailed December 22, 2004, claims 4-26. 28-45 and 58-60 were allowed. Claims 49, 53, and 57 were indicated as allowable if rewritten independently to contain all limitations in their base claims and an any intervening claim(s). Claims 46-48, 50-52 and 54-56 were rejected on grounds each element of those claims was shown in US 6,526,430 of Huang et al.

Reconsideration and allowance are requested in view of the following remarks.

The cited reference does not show or suggest the subject matter of claim 46. That is an independent claim and all other rejected claim ultimately depend from claim 46. The following remarks will show that claim 46 is patentable over the applied art in US 6,526,430 of Huang et al.

Claim 46 defines three networks: a network of multipliers, another of adders and another of accumulators. A plurality of control switches coupled to the multipliers operate to connect the outputs of the multipliers to either the array of adders or the array of accumulators. In this way, the claimed invention may rapidly switch between two different but desired types of multiplications: conventional and matrix.

The features of claim 46 are illustrated in Fig. 28 of the application. There one sees the array of multipliers that may have their outputs connected to the adder

arrays to perform conventional multiplication or switched to the accumulator arrays to provide matrix multiplication. The invention thus has the unique ability to switch its functional multiplier units from conventional multiplication to matrix multiplication without the necessity of reprogramming the device or reconfiguring the functional elements. No reconfiguration is required because the structure for performing both conventional and matrix multiplication is already in place in the invention.

In contrast, the applied art does not have the claimed arrays and switches. Instead, the cited art may be reconfigured by suitable programming to reconfigure and/or connect its functional components into different configurations for carrying out different operations. But there is not express teaching of the using the same multiplier array to perform both conventional and matrix multiplication. The cited art requires reprogramming or structural reorganization to achieve different results. But it does not have one set of multipliers that is switched between two output arrays for switching the computation between conventional and matrix multiplication.

In particular, the Huang reference does not show control switches connected between multipliers and arrays of adders or accumulators. The rejection relies upon Col. 9, lines 57-62. However, that section makes no mention of switches. It merely states that different tasks are assigned as required. It does not show the claimed switches.

The Huang reference does not show switching the outputs of multipliers between an array of adders and an array of accumulators. Huang, to be sure, shows multipliers, adders and accumulators as elements. But in each instance the arrangement is nearly identical: multipliers feed into adders and the outputs of adders (as expected) go to accumulators. The reference does not show an instance of where the output of the multiplier goes to an accumulator before going to an adder. As such, the reference fails to show or suggest the disjunctive connection of a multiplier array to either an array or accumulators or to an array of adders because its multipliers are always connected to adders and not to accumulators.

A notice of allowance is respectfully requested.

Respectfully submitted,

4/15/2005
Date

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